

Appl. No. 09/432,687  
Amdt. dated August 18, 2003  
Reply to Office Action of June 18, 2003

CURRENTLY PENDING CLAIMS

The listing of claims below replace all prior versions, and listings, of claims:

- 1           1.       (Original) A semiconductor device, comprising:  
2                   memory cells each having an area of about  $6F^2$ ;  
3                   sense amplifiers;  
4                   bit lines coupled to the sense amplifiers in a folded bit line configuration, each bit  
5 line including a first level portion and a second level portion; and  
6                   active area lines, transistors being formed in the active area lines and electrically  
7 coupling corresponding memory cells to corresponding first level bit lines.
- 1           2.       (Original) The semiconductor device of claim 1, wherein each pair of bit lines is  
2 vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning  
3 between the first level portion and the second level portion at each twist.
- 1           3.       (Original) The semiconductor device of claim 2, wherein a column pitch of each  
2 memory cell is  $2F$ .
- 1           4.       (Original) The semiconductor device of claim 1, wherein each memory cell  
2 includes a capacitor formed over the first level portion of each bit line.
- 1           5.       (Original) The semiconductor device of claim 4, wherein the second level portion  
2 of each bit line is formed over each capacitor.
- 1           6.       (Original) The semiconductor device of claim 1, wherein the bit lines extend  
2 generally along the same direction as the active area lines, the bit lines intersecting the active  
3 area lines at slanted portions,  
4                   the semiconductor device further comprising contacts between the bit lines and  
5 active area lines formed in the slanted portions.

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1           7.       (Original) The semiconductor device of claim 6, wherein the active area lines are  
2 generally straight and the bit lines extend in a wavy pattern.

1           8.       (Original) The semiconductor device of claim 6, wherein the bit lines are  
2 generally straight and the active area lines extend in a wavy pattern.

1           9.       (Original) The semiconductor device of claim 6, each bit line having a first  
2 portion on a first side of a corresponding active area line, a second portion on a second side of  
3 the corresponding active area line, and a third portion on the first side of the active area line.

1           10.      (Original) The semiconductor device of claim 6, wherein the bit lines extend  
2 along generally the same direction as the active area lines so that the bit lines and active area  
3 lines intersect at predetermined locations.

1           11.      (Original) A memory device comprising:  
2                   memory cells each having an area of about  $6F^2$ ;  
3                   sense amplifiers;  
4                   bit lines coupled to the sense amplifiers in a folded bit line arrangement;  
5                   active area lines; and  
6                   transistors formed in the active area lines and electrically coupling corresponding  
7 memory cells to corresponding bit lines.

1           12.      (Original) The memory device of claim 11, wherein each bit line has a first level  
2 portion and a second level portion, each transistor electrically coupling a corresponding memory  
3 cell to a first level portion of a corresponding bit line.

1           13.      (Original) The memory device of claim 12, wherein each pair of bit lines is  
2 vertically twisted at one or more predetermined locations, the bit lines in the pair transitioning  
3 between the first level portion and the second level portion at each twist.

1           14.    (Original) The memory device of claim 12, wherein each memory cell includes a  
2    capacitor formed over the first level portion of each bit line.

1           15.    (Original) The memory device of claim 14, wherein the second level portion of  
2    each bit line is formed over each capacitor.

1           16.    (Original) The memory device of claim 11, wherein the bit lines extend generally  
2    along the same direction as the active area lines, the bit lines intersecting the active area lines at  
3    slanted portions.

1           17.    (Original) The memory device of claim 11, wherein each pair of bit lines is  
2    coupled to one side of a corresponding sense amplifier.

1           18.    (Original) A method of making a memory device, comprising:  
2                   forming memory cells each having an area of about  $6F^2$ ;  
3                   forming sense amplifiers;  
4                   coupling bit lines to the sense amplifiers in a folded bit line arrangement;  
5                   forming transistors in active area lines; and  
6                   the transistors electrically coupling corresponding memory cells to corresponding  
7    bit lines.

1           19.    (Original) The method of claim 18, further comprising:  
2                   forming each bit line of a first level portion and a second level portion; and  
3                   coupling each transistor to the first level portion of the corresponding bit line.

1           20.    (Original) The method of claim 19, further comprising:  
2                   vertically twisting each pair of bit lines at one or more predetermined locations;  
3    and  
4                   transitioning the bit lines in the pair between the first level portion and the second  
5    level portion at each twist.

1           21.    (Original) The method of claim 20, further comprising forming a capacitor of  
2   each memory cell over the first level portion of each bit line.

1           22.    (Original) The method of claim 21, further comprising forming the second  
2   level portion of each bit line over the capacitor.

1           23.    (Previously Presented) The semiconductor device of claim 1, wherein in  
2   the folded bit line arrangement a pair of bit lines is coupled to a same side of each  
3   corresponding sense amplifier.

1           24.    (Previously Presented) The memory device of claim 11, wherein in the  
2   folded bit line arrangement a pair of bit lines is coupled to a same side of each  
3   corresponding sense amplifier.

1           25.    (Previously Presented) The method of claim 18, wherein coupling the bit  
2   lines to the sense amplifiers in the folded bit line arrangement comprises coupling each  
3   pair of bit lines to a same side of each corresponding sense amplifier.